

WHAT IS CLAIMED IS:

1. An information handling system, comprising:
memory;
at least one processor operably associated with the
5 memory;
a printed circuit board operable to maintain the
processor and the memory;
a plurality of vias disposed in at least one printed
circuit board layer, the vias defined by a first opening
10 on a first surface of the printed circuit board layer, a
second opening at a second surface of the printed circuit
board layer and at least one side wall connecting the
first and second openings and defining a void
therebetween; and
15 a conductive material disposed on a portion of the
side wall, the conductive material defining at least one
inner-via trace.
2. The information handling system of Claim 1,
20 further comprising the inner-via trace having a total
impedance substantially approximating a printed circuit
board surface mounted trace impedance.
3. The information handling system of Claim 1,
25 further comprising:
the conductive material disposed in the void
defining a plurality of inner-via traces, and
the plurality of inner-via traces arranged in a
striped pattern, where the patterned stripes travel
30 between the first opening and second opening.

4. The information handling system of Claim 1, further comprising a conductive pad disposed on the first surface of the printed circuit board layer and proximate the first opening and coupled to the inner-via traces.

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5. The information handling system of Claim 4, further comprising a conductive pad disposed on the second surface of the printed circuit board layer and proximate the second opening and coupled to the inner-via traces.

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6. The information handling system of Claim 1, further comprising a conductive trace disposed on the first surface of the printed circuit board layer and coupled to the inner-via traces.

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7. The information handling system of Claim 6, further comprising a conductive trace disposed on the second surface of the printed circuit board layer and coupled to the inner-via traces.

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8. The information handling system of Claim 1, further comprising:

a printed circuit board having a plurality of layers; and

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at least one via disposed through a first layer and terminating proximate a first surface of a second layer.

9. A method for manufacturing an electronic component substrate, comprising:

defining an aperture in a first substrate layer, the aperture including a first opening at a first surface of the substrate layer, a second opening at a second surface of the substrate layer and a barrel defined by at least one side wall creating a void and traveling between the first and second openings; and

creating an inner-void trace on a portion of the barrel side wall and traveling between the first and second surfaces, the inner-void trace coupling a first trace on the first surface of the substrate layer to a second trace on the second surface of the substrate layer.

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10. The method of Claim 9, further comprising creating multiple inner-void traces and leaving non-trace regions of the barrel side-wall substantially devoid of conductive material.

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11. The method of Claim 9, further comprising:
disposing at least one layer of conductive material on the barrel side wall; and

removing portions of the conductive material from the barrel side wall, leaving only a layer of conducting material forming an inner-void trace.

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12. The method of Claim 9, further comprising
substantially balancing at least one electrical
characteristic of the inner-void trace to a corresponding
electrical characteristic of the first and second surface
5 traces.

13. The method of Claim 9, further comprising
substantially balancing an impedance value of the inner-
void trace with an impedance value of the first and
10 second surface traces.

14. The method of Claim 9, further comprising
disposing a second substrate layer on a surface of the
first substrate layer thereby forming a multi-layered
15 electronic component substrate.

15. An apparatus, comprising:
at least one substrate having a first surface and a second surface;
a first conductive trace disposed proximate the
5 first surface of the substrate;
a second conductive trace disposed proximate the second surface of the substrate;
at least one via disposed in the substrate, the via defining an aperture in the substrate traveling from the
10 first surface to the second surface; and
at least one conductive inner-via trace operably coupled to the via, the inner-via trace operably coupling the first conductive trace to the second conductive trace and having at least one electrical characteristic
15 substantially approximating a corresponding electrical characteristic of a substrate surface conductive trace.
16. The apparatus of Claim 15, further comprising the inner-via trace having an impedance measure
20 substantially approximating an impedance measure of the first and second conductive surface traces.
17. The apparatus of Claim 15, further comprising:
the substrate having a plurality of layers; and
25 the first conductive trace disposed between a first pair of substrate layers and the second conductive trace disposed between a second pair of substrate layers.

18. The apparatus of Claim 15, further comprising:
the substrate having a first plurality of layers;
and

the first conductive trace disposed on an external
5 surface of the plurality of substrates and the second
conductive trace disposed between adjacent layers of the
plurality of substrates.

19. The apparatus of Claim 15, further comprising:
10 a plurality of conductive inner-via traces; and
the plurality of conductive inner-via traces
collectively having at least one electrical
characteristic substantially approximating a
corresponding electrical characteristic of a substrate
15 surface conductive trace.

20. The apparatus of Claim 19, further comprising
an impedance total for the plurality of inner-via traces
substantially approximating that of the first surface
20 conductive trace and the second surface conductive trace.